



Application No.: 09/739,956  
Art Unit: 2671

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Examiner: Arnold, A.

Claim 1

- 1) Where does Murphy discuss a calculation circuit (e.g., hardware) configured to calculate an address in a second address range for storage of data corresponding to pixels?
- 2) Where does Murphy discuss a control circuit configured to control writing of data in a memory across a bus by driving an address onto the bus?
- 3) What in FIG. 5D of Murphy and in column 62, line 7 of Murphy shows driving an address onto a bus?
- 4) How does the answer for 3) reconcile with the statement "As pointed out in the previous action, there are no addresses on the bus; it is merely a wire for transporting data." (Office Action, page 10, lines 2-3, emphasis added.)?

Claim 15: How does Ozcelik teach "increased" flexibility in defining displays as compared with Murphy?

Claim 3: Where does Murphy discuss a clipping circuit generating a clipping signal to indicate that at least one coordinate falls outside a predetermined clipping limit?

Claims 4 and 21:

- 1) Why is inhibiting a write operation inherent?
- 2) How is the inherency responsive to the clipping signal?

Claim 5: Where do the arguments for claim 4 discuss inhibiting writing to an address?

Claim 6: Where do the arguments for claim 4 discuss preventing address calculations?

Claims 7 and 22: Why does a register having an associated address tag mean that the register has more than one memory location?

Claim 8

- 1) Where does Chiu discuss the address decoder 206 monitoring address locations?
- 2) Where does Chiu discuss a control unit?
- 3) Where does Chiu discuss the address decoder 206 applying a location signal to the control unit of Chiu representative of the address location being written to?

Claim 9: Where do the arguments for claims 1 and 8 discuss that the control circuit of Murphy is configured to control a first and a second register and a calculation circuit?

Claim 10: Where do the arguments for claims 1 and 8 discuss that the control circuit of Murphy instructs a calculate circuit to calculate an address in response to writing to one of four locations between two registers?

Claim 14: Where do the arguments for claims 8 and 11 discuss that:  
1) two registers can be mapped to eight different locations?  
2) the address decoder of Chui monitors the eight locations?  
3) the address decoder of Chui generates a location signal representative of address location being written to?  
4) the address decoder of Chui indexes a style counter in response to the address location being written to?

Claim 16: What in FIG. 2B of Murphy is similar to the claimed logic circuit?

Claim 17: How does a multiplexer combine two data items into a single memory word?

Claim 18: How does comparing pixel addresses "preserve physical memory"?

Claim 19: Where do the arguments for claims 1 and 18 discussed that the control circuit of Murphy combines data for pixels in response to a receipt of the same address signal?

Claim 23: Where do the arguments for claims 8 and 22 discuss monitoring four locations between two registers for a write?

Claim 24: Where do the arguments for claims 8 and 22 discuss calculating an address for a pixel in response to the write to one of the four locations?

Claim 27: Where do the arguments for claims 17 and 20 discuss storing data in a single memory word prior to writing the single memory word to the memory?

Claim 28: Where do the arguments for claims 15 and 20 discuss combining data for at least two pixels to permit storage in a single memory word?

Claim 29:

- 1) Where do the arguments for claims 18 and 20 discuss comparing word addresses of consecutive pixels?
- 2) Where do the arguments for claims 18 and 20 discuss combining data if their word addresses are identical?

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